PRIFYSGOL CYMRU; UNIVERSITY OF WALES

M.Sc. AND DIPLOMA EXAMINATIONS

JANUARY 2003

SWANSEA

Computer Science

CS M33   Computer Systems

Attempt 2 questions out of 3

Time allowed: 2 hours

Students are permitted to use the dictionaries provided by the University

Students are NOT permitted to use calculators

COMPUTER SYSTEMS
*(**Attempt** 2 **questions out of** 3)*

Question 1.

(a) Draw a circuit, which determines the result of the following Boolean expression

$$\overline{x} \cdot y \cdot z + x \cdot \overline{y} \cdot z + x \cdot y \cdot \overline{z}$$

depending on inputs x, y, z.

[4 marks]

(b) (i) Determine a Boolean formula which, depending on variables x, y, z, has result f(x,y,z), where f is given by the following table:

x	y	z	f(x,y,z)
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	1

(ii) Try to improve your solution in (i), so that it requires as few logical operations as possible.

[6 marks]

(c) Construct a 4-way multiplexer from simple (2-way) multiplexers. A 4-way multiplexer has as input 2 control signals c_0, c_1 and 4 input lines a_0, a_1, a_2, a_3. Depending on the control signals one of the input lines is selected as output. Further for each input line there exists control signals c_0, c_1 which select this input line as output. (Hint: First use 2-way multiplexers to select out of a_0, a_1 and out of a_2, a_3 one each; then use one 2-way multiplexer to select out of these two groups one output).
Explain your solution, for instance by drawing a truth table which determines the outputs of each of your multiplexers depending on the control signals. **[6 marks]**

(d) Draw the configuration of an R-S-latch. Which outputs represent memory value 0? Which inputs are used in order to store this memory value in it? Describe, possibly using a table, how the R-S-latch adapts when the inputs for storing memory value 0 are applied to it. The state of the R-S latch before setting these inputs is supposed to be unknown.

[9 marks]

Question 2.

(a) How many bits are in one kilobyte? It suffices to express your result by a formula.

[**2 marks**]

(b) Why does DRAM require refreshing? Which problems are caused by this?

[**3 marks**]

(c) (i) Assume a direct mapped cache with 4 blocks of 2 bytes each, which is initially empty. Assume that a series of load requests from main memory is carried out. The byte level addresses of these in decimal representation are: 0, 1, 2, 0, 9, 0. Determine for each reference, whether it is a hit or a miss, and the main memory addresses of the blocks stored in each cache line after the corresponding load operation has been carried out.

(ii) Answer the same questions as in (i), if the cache has a size of 8 bytes, a block size of 2 bytes, and is set-associative with 2 lines per set.

[**12 marks**]

(d) Assume a fully associative cache of four bytes with block size 1 byte, which is initially empty. Assume that the following sequence of memory load requests is carried out, given as byte addresses: 1, 2, 1, 1, 1, 2, 3, 3, 3, 4, 4, 4, 4, 3, 2, 1, 5. When the last address 5 is to be loaded, the cache is full and one line in cache has to be replaced. There are four main algorithms for determining, which block in the cache is to be replaced. Describe each of them briefly, and the main memory address of the block, which will be overwritten (if there is more than one possibility, determine all of them).

[**8 marks**]

Question 3.

(a) Describe the basic structure of the von Neumann machine. You might make use of a diagram.

[2 marks]

(b) Assume an architecture with a word length of 16 bits, 16 bit addresses which refer to words, one 16 bit register R and a program counter PC. Assume that the registers and the following memory addresses have at the moment when we start to calculate the operands below, the following content:

Register/Memory address	Content
R	0x0300
PC	0x03F0
0x0300	0x0310
0x0310	0x0320
0x0320	0x0330
0x0330	0x0340

Calculate the operand given by the following addresses and addressing modes:

   (i) immediate addressing 0x0310,

  (ii) indirect addressing 0x0310,

 (iii) direct addressing 0x0310,

 (iv) register indirect addressing R,

  (v) relative addressing 0x0310.

Explain in each case, how the operand is calculated.

[10 marks]

(c) Assume a processor with one register called AC, no other user visible registers, and the following commands (which refer to integer data):

Command	Explanation
LOAD A	Load content at memory address A into AC.
STORE A	Store content of AC into main memory at address A.
ADD A	Add content of memory location A to the content of AC, store result in AC.
MULT A	Multiply content of memory location A with content of AC, store result in AC.

Assume that variables a, b, c are stored at memory addresses A, B, C. Translate the following command of a higher programming language into assembler code for this processor:

$$a := (b + c) * a$$

($*$ is multiplication, and $:=$ is the assignment of a value to the variable on the left side of $:=$).

[4 marks]

(d) Assume an architecture, having one general purpose register AC, an instruction register (IR) and a program counter (PC). The architecture should have a word size of 2 bytes, and addresses should refer to word level. Assume that the instruction set has an instruction STORE A, meaning "store the word in register AC into memory location A". Assume an address length of 12 bits, and that instructions are encoded as 16 bits. The leftmost 4 bits of the instruction code determine the type of instruction (where 0x1 means STORE) and the remaining 12 bits form the address. So 0x1700 encodes STORE 700. Both AC and IR store 2 bytes and the PC stores 12 bits. Assume the following content of main memory

Address	Content
0x400	0x1700
0x700	0x1700

and of the registers

Register	Content
PC	0x400
AC	0x0400
IR	0x0400

Assume that the CPU is about to fetch the instruction with address given in the PC. Describe the content of the registers (AC, IR and PC) and of the main memory locations 0x400 and 0x700 after the fetch- and after the execution-cycle for this instruction. Explain the movement of data between the registers and main memory during these cycles.

[9 marks]